Claims

[c1] An integrated memory device, comprising:
a memory cell array having a plurality of memory cells interconnected by wordlines and bitlines, the bitlines of the memory array are arranged in pairs including a first and a second bitline;
a plurality of sense amplifiers coupled to the bitlines, wherein a sense amplifier is coupled to a bitline pair;
a data line, the plurality of sense amplifiers are multiplexed to the data line, the data line transmitting information from a selected cell from one of the plurality of sense amplifiers; and
a data line precharge circuit coupled to the data line, the data line precharge circuit, when activated, precharges the data line to a data line reference voltage.

[c2] The integrated memory device of claim 1 wherein the data line reference voltage is about $V_{DD}/2$.

[c3] The integrated memory device of claim 1 wherein the data line reference voltage is about $V_{DD}/2+\Delta V$.

[c4] The integrated memory device of claim 1 wherein the data line reference voltage is about V_{SS}.

[c5] The integrated memory device of claim 1 wherein the data line precharge circuit comprises a voltage source, the voltage source being selectively coupled to the data line using a switching element.

[c6] The integrated memory device of claim 5 wherein the switching element comprises a transistor.

[c7] The integrated memory device of claim 5 wherein the data line precharge circuit is activated by a precharge signal.

[c8] An integrated memory device, comprising:
a plurality of memory cells and a plurality of bitlines, a memory cell being connected to one of said bitlines;
a plurality of sense amplifiers, a sense amplifier being connected to a first and a

second one of said bitlines;

an output of each one of said sense amplifiers being coupled to a data line through a first switching element; and

a second switching element coupling said data line to a reference voltage source.

[c9] The memory device of claim 8, wherein said first switching element is inactive when said second switching element is active, and wherein said first switching element is active when said second switching element is inactive.

[c10] The memory device of claim 9, wherein said first switching element comprises a transmission gate.

[c11] The memory device of claim 10 wherein said second switching element comprises a transistor.

[c12] The memory device of claim 8 wherein the reference voltage source provides a reference voltage of about $V_{DD}/2$.

[c13] The memory device of claim 8 wherein the reference voltage source provides a reference voltage of about $V_{DD}/2+\Delta V$.

[c14] The memory device of claim 8 wherein the reference voltage source provides a reference voltage of about V_{SS}.